JHARKHAND Rai University
UGC RECOGNISED UNIVERSITY
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Lesson Plan & Tracking

Programe : B. Tech (CSE) | **Session : 2021 - 2024** | **Year : 2021** | **Sem: 3rd**

Course: Computer Organization & Architecture(Theory)

Name of the Faculty: Rajan Kumar Tiwari | **Commencement Date: 29.08.2022** | **Date of Closure: 30.12.22**

Lecture No.	Week	Unit	Topics to be Covered	Blended Mode			Date	Duration	Tracking of Lectures	Related Course Outcome	Signature of Faculty	Signature of HoD	Remarks (if any)
				ICT Tool/Platform/ LMS	Resources	Activity							
1	1	1	To discuss course objective-outcome and syllabus of COA										
2		1	Overview of Functional blocks of a computer										
3		1	control unit. Instruction set architecture of a CPU										
4	2	1	registers, instruction execution cycle,										
5		1	instruction set, addressing modes, RTL interpretation of instructions										
6		1	addressing modes										
7	3	1	addressing modes										
8		1	instruction sets of some common CPUs										
9		1	Signed number representation										
10	4	1	fixed and floating point representations, character representation										
11		1	Computer arithmetic – integer addition and subtraction										
12		1	ripple carry adder, carry look- ahead adder										
13	5	1	Booth multiplier										
14		1	Division restoring and non-restoring techniques										
15		1	floating point arithmetic										
16	6	2	Introduction to x86 architecture										
17		2	hardwired desogn approach										
18		2	micro- programmed design										
19	7	2	semiconductor memory technologies										
20		2	memory organization										
21		2	Peripheral devices: Input-output subsystems										
22		2	I/O device interface, I/O transfers–program controlled										

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23	8	2	DMA										
24		2	privileged and non- privileged instructions, software interrupts and exceptions										
25	9	2	role of interrupts in process state transitions, SCII, USB										
26		3	Basic concepts of pipelining, throughput and speedup										
27		3	pipeline hazards										
28	10	3	Introduction to parallel processors, Concurrent access to memory										
29		3	Cache coherency										
30		4	Memory interleaving, concept of hierarchical memory organization,										
31	11	4	cache memory, cache size vs. block size										
32		4	mapping functions										
33		4	cache write policies										
34	12	4	cache replacement algorithms										
35			Model paper discussion										
36			Model paper discussion										